termination structure may be provided on an outermost peripheral portion of the device.

[0103] This application claims priority based on Japanese Patent Application No. 2011-092962 filed on Apr. 19, 2011, and the contents of this application are incorporated in the specification of the present invention by reference.

INDUSTRIAL APPLICABILITY

[0104] In accordance with the present invention, the anode region is formed in the bottom portion of the trench in which the gate electrode is formed or in the drift region immediately under the trench. Accordingly, with respect to the gate electrode, the diode can be formed in the vertical direction of the substrate. As a result, the area efficiency of the element in the semiconductor substrate is enhanced, whereby the integration degree can be enhanced.

1-12. (canceled)

13. A semiconductor device comprising:
- a semiconductor substrate;
- a drift region of first conductivity type formed on one of main surfaces of the semiconductor substrate;
- a well region of second conductivity type formed in the drift region;
- a source region of first conductivity type formed in the well region;
- a trench with a depth penetrating the source region and the well region and reaching the drift region;
- a gate electrode formed on a side portion of the trench while interposing a gate insulating film therebetween;
- a source electrode connected to the well region and the source region;
- a drain electrode connected to other of the main surfaces of the semiconductor substrate;
- an interlayer insulating film that is formed on the gate electrode and coats the gate electrode;
- an anode region formed on a bottom portion of the trench or in the drift region immediately under the trench;
- a contact hole formed at a depth reaching the anode region in the trench; and
- an inner wall insulating film formed on an inner wall side surface of the contact hole while being in contact with the gate electrode,
- wherein the source electrode is embedded in the contact hole while interposing the inner wall insulating film between the source electrode and the gate electrode, and is electrically connected to the anode region in a state of being insulated from the gate electrode by the inner wall insulating film, and
- a plurality of the contact holes is formed discretely in the trench with respect to a main surface direction of the semiconductor substrate, and a width of the trench at portions in which the contact holes are formed is wider than a width of the trench at portions in which the contact holes are not formed.

14. The semiconductor device according to claim **13**, wherein the anode region is formed as a second conductivity type region in the drift region, and composes a PN junction-type diode on a junction surface with the drift region, the PN junction-type diode using the drift region as a cathode.

15. The semiconductor device according to claim **13**, wherein the anode region is formed of a material different from the drift region on the bottom portion of the trench, and composes a unipolar diode on a junction surface with the drift region.

16. The semiconductor device according to claim **15**, wherein the anode region is formed of a semiconductor different in band gap from the drift region.

17. The semiconductor device according to claim **13**, wherein a plurality of the trenches is formed linearly with respect to the main surface direction of the semiconductor substrate, and a plurality of the contact holes is formed discretely in the trenches with respect to the main surface direction of the semiconductor substrate, and the contact holes formed in the trenches adjacent to one another are arranged and formed alternately so as not to be opposite to one another.

18. A semiconductor device comprising:
- a semiconductor substrate;
- a drift region of first conductivity type formed on one of main surfaces of the semiconductor substrate;
- a well region of second conductivity type formed in the drift region;
- a source region of first conductivity type formed in the well region;
- a trench with a depth penetrating the source region and the well region and reaching the drift region;
- a gate electrode formed on a side portion of the trench while interposing a gate insulating film therebetween;
- a source electrode connected to the well region and the source region;
- a drain electrode connected to other of the main surfaces of the semiconductor substrate;
- an interlayer insulating film that is formed on the gate electrode and coats the gate electrode;
- an anode region formed on a bottom portion of he trench or in the drift region immediately under the trench;
- a contact hole formed at a depth reaching the anode region in the trench; and
- an inner wall insulating film formed on an inner wall side surface of the contact hole while being in contact with the gate electrode,
- wherein the source electrode is embedded in the contact hole while interposing the inner wall insulating film between the source electrode and the gate electrode, and is electrically connected to the anode region in a state of being insulated from the gate electrode by the inner wall insulating film, and
- the anode region is formed of a semiconductor different in band gap from the drift region.

19. The semiconductor device according to claim **18**, wherein the trenches are formed into a mesh shape with respect to the main surface direction of the semiconductor substrate, and a plurality of the contact holes is arranged and formed discretely on mesh intersections of the trenches.

20. The semiconductor device according to claim **18**, wherein the trench is formed linearly with respect to a main surface direction of the semiconductor substrate, and the contact holes are formed linearly along an inside of the trench.

21. The semiconductor device according to claim **18**, wherein the trench is formed into a mesh shape with respect to a main surface direction of the semiconductor substrate, and the contact holes are formed into a mesh shape along an inside of the trench.

* * * * *